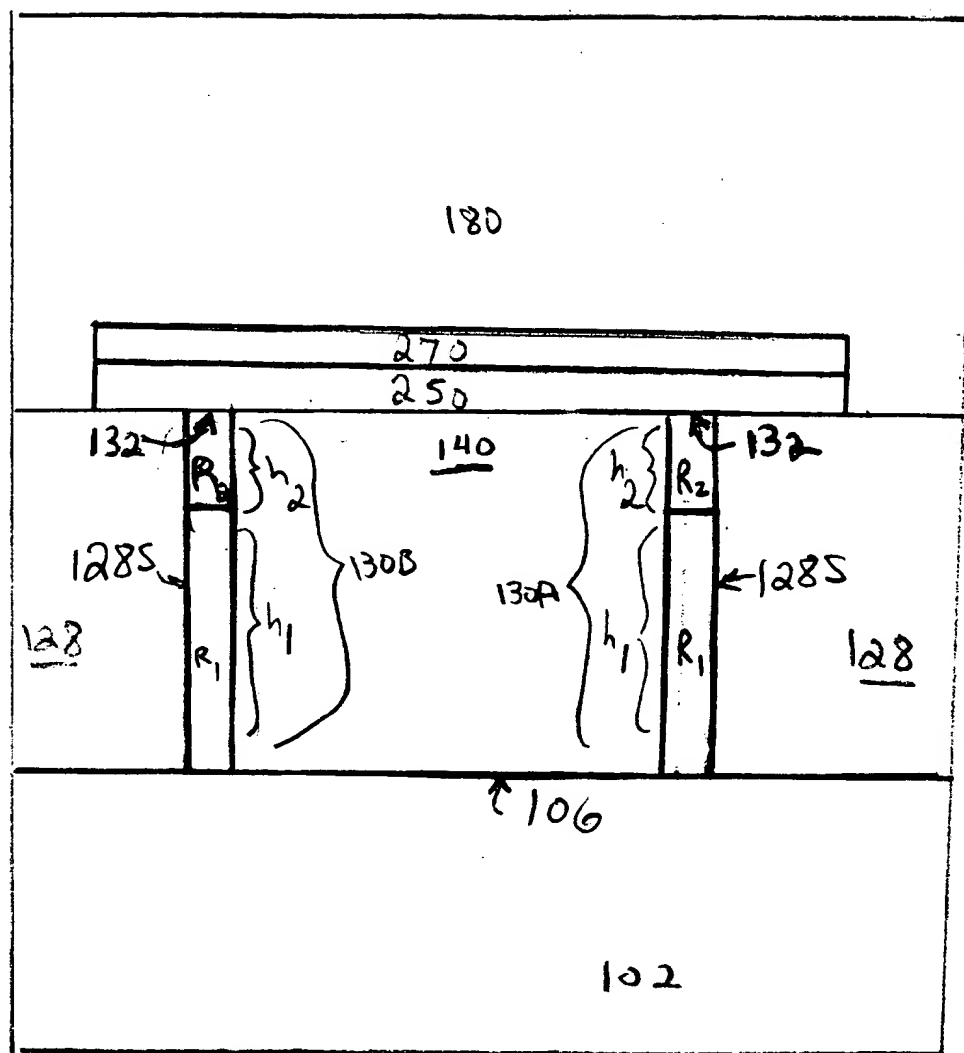


0960318-07200



← CHANNEL LENGTH →

↑  
100

FIGURE 1A

A perspective view of a channel 102. The channel has a bottom layer 102, side walls 128, and a top layer 132. The top layer 132 is divided into two sections, 130A and 130B, by a vertical dashed line. The width of the channel is labeled as 'CHANNEL WIDTH' with an arrow pointing to the right. The length of the channel is labeled as 'CHANNEL LENGTH' with an arrow pointing to the left. The height of the side walls is labeled 'h' with a bracket. The thickness of the top layer 132 is labeled 't' with a bracket. The angle between the top layer 132 and the side walls 128 is labeled '130A' and '130B'.

FIGURE 1B

FIGURE 1C



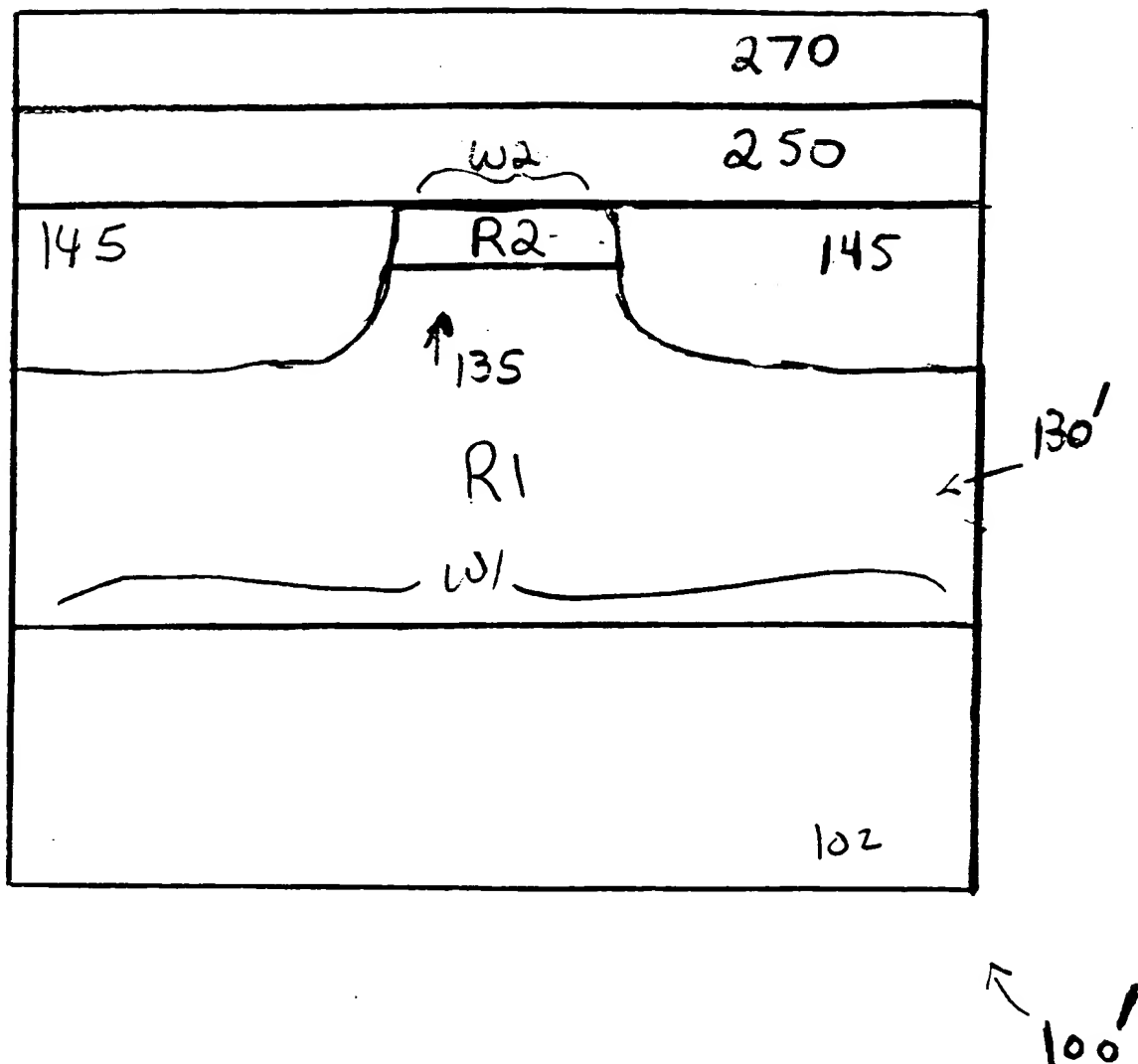


FIGURE 1E

180

270  
280  
280

132  
1285  
128

$R_1$

130A

140

130B

$R_2$

132  
1285  
128

$R_1$

106

102

100

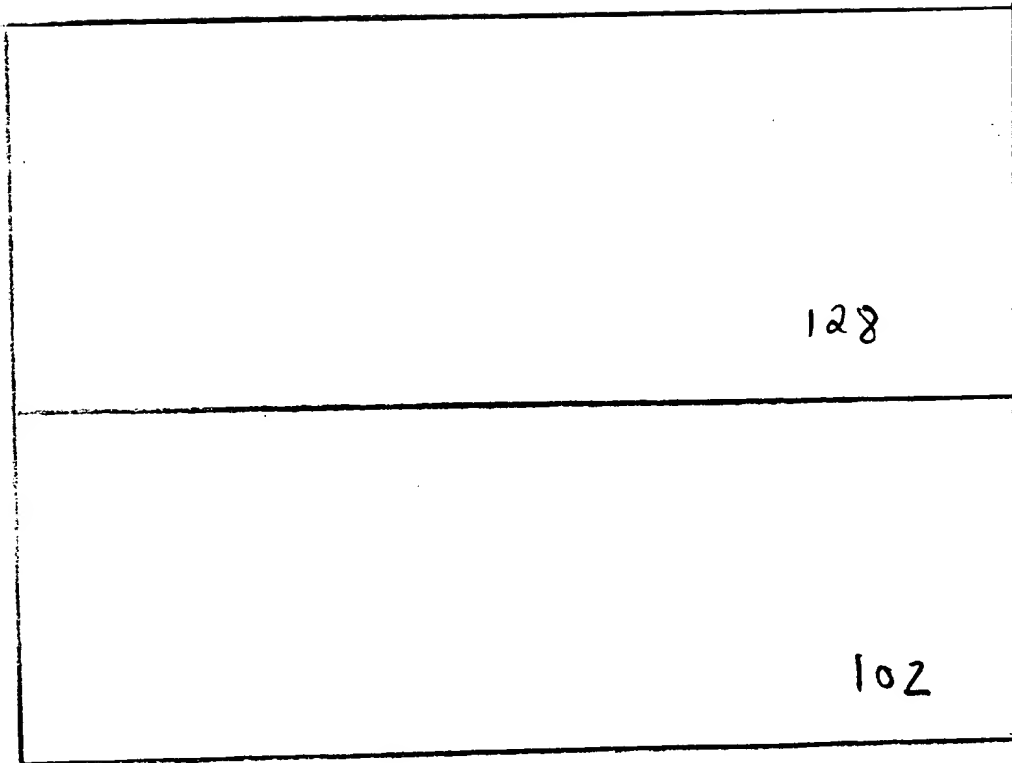
FIGURE 1 F

Hand-drawn schematic diagram of a multi-layer PCB layout. The diagram shows a top layer with dimensions 180, 270, and 250. Below this is a core or prepreg layer with dimensions 140 and 106. The core/prepreg layer is divided into two vertical sections, 130A and 130B, each containing three horizontal layers labeled R1, R2, and R3. Dimensions 132, 128, and 1285 are indicated for these layers. The bottom layer is labeled 102.

100

FIGURE 1G

05000348-072000



↑  
200A

FIGURE 2A



0960318 070000

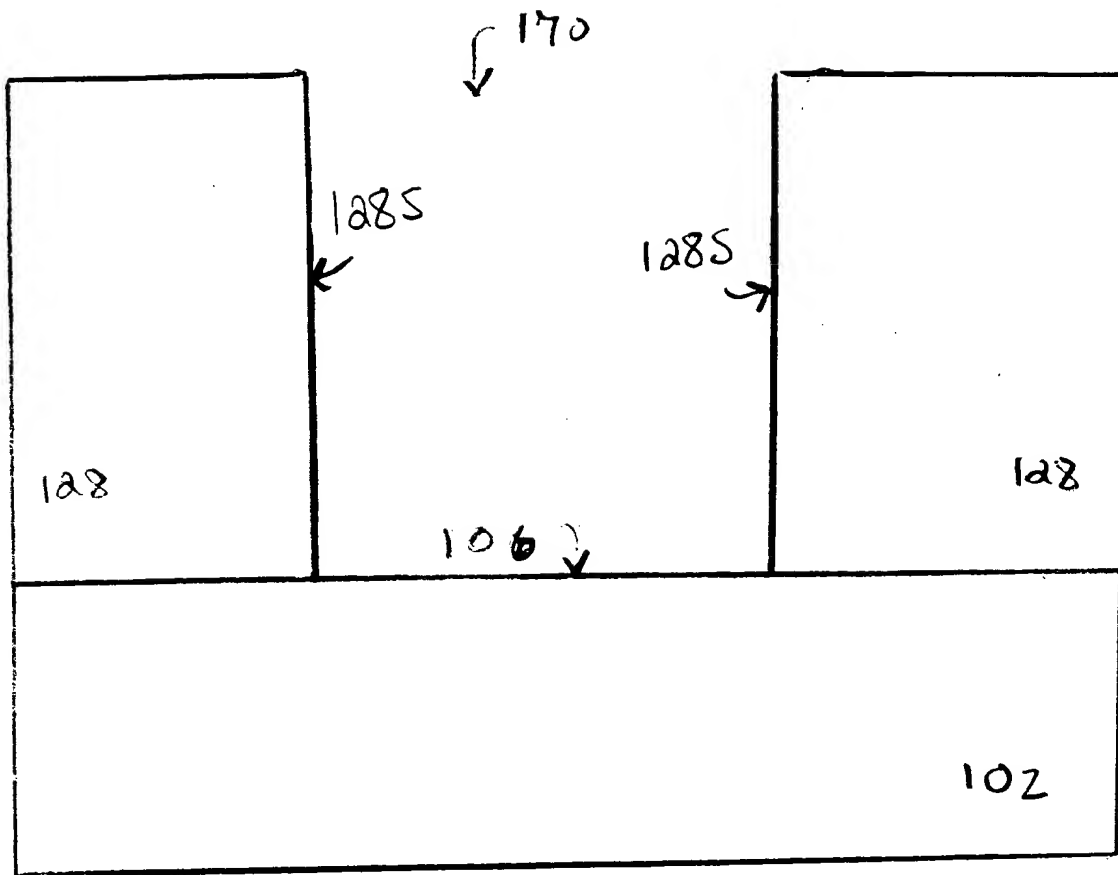


FIGURE 2B

0960348 072000

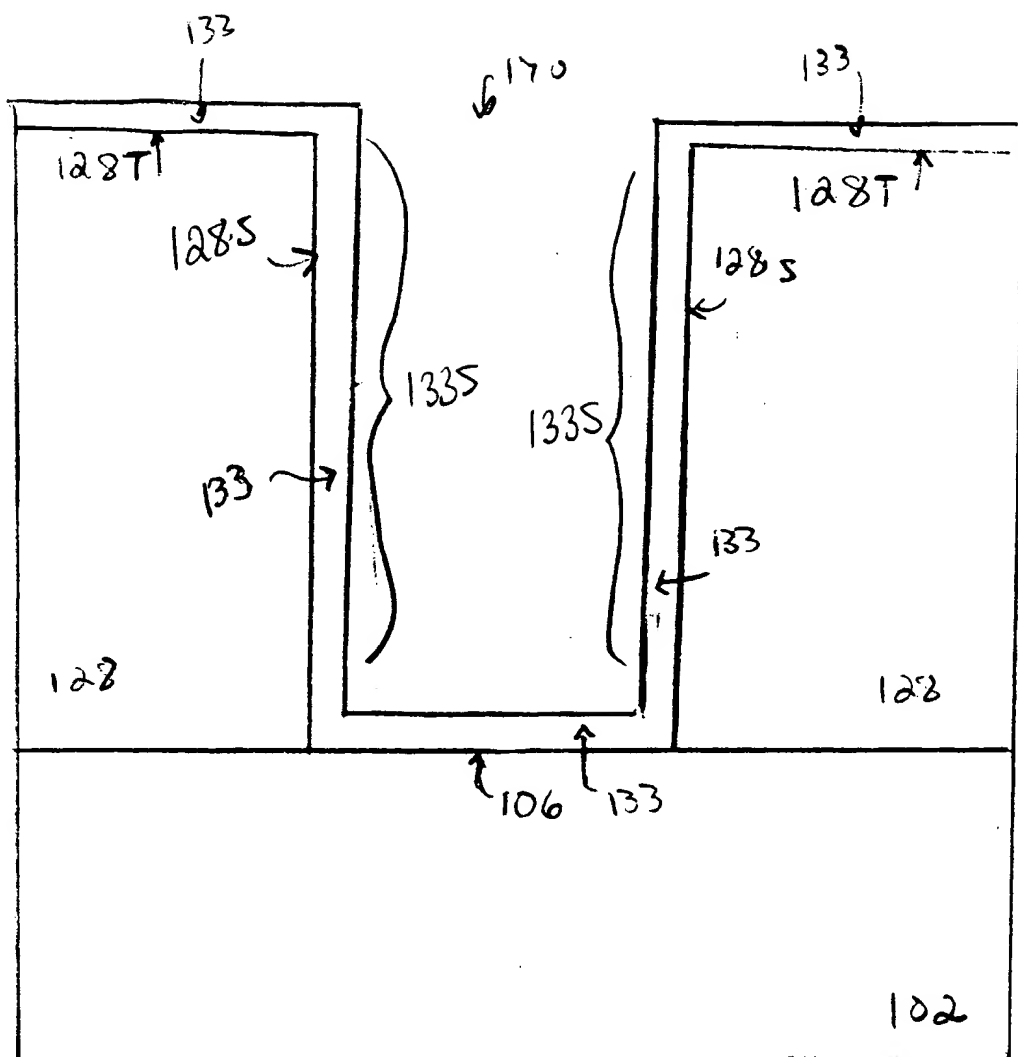


FIGURE 2C

0560318 07P00

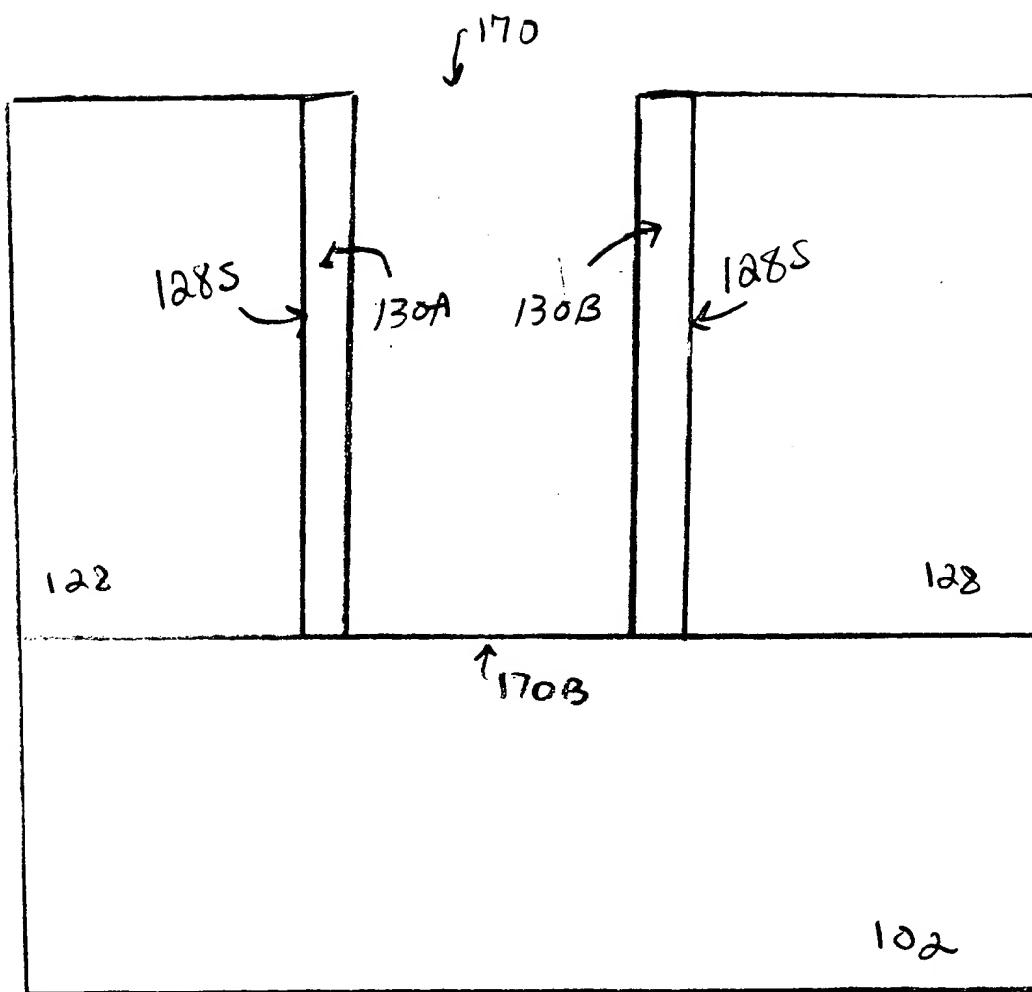


FIGURE 2D

Hand-drawn schematic diagram of a multi-layer PCB layout. The diagram shows a central rectangular area labeled '140' with two vertical strips on either side, labeled '130A' and '130B'. The top and bottom edges of the central area are labeled '140'. The left and right edges of the vertical strips are labeled '128'. The bottom edge of the entire assembly is labeled '102'. Arrows point from the labels '130A' and '130B' to the respective vertical strips.

FIGURE 2E

A hand-drawn schematic diagram of a 2D grid. The grid is divided into four quadrants by a horizontal line and a vertical line. The top-left quadrant is labeled '128'. The top-right quadrant is labeled '128'. The bottom-left quadrant is labeled '102'. The bottom-right quadrant is labeled '102'. In the center of the grid, there is a label '140'. To the left of the center, there is a label 'R1' with an arrow pointing left towards the label '130A'. To the right of the center, there is a label 'R2' with an arrow pointing right towards the label '130B'. At the top of the grid, there are two labels '132' with arrows pointing down towards the top edge of the grid.

↑  
200F

FIGURE 2F



		270	
		250	
<div> <div>132</div> <div> <div><math>R_2</math></div> <div><math>R_1</math></div> </div> <div>130A</div> <div>128</div> </div>	140	<div> <div>132</div> <div> <div><math>R_2</math></div> <div><math>R_1</math></div> </div> <div>130B</div> <div>128</div> </div>	
102			

FIGURE 2H

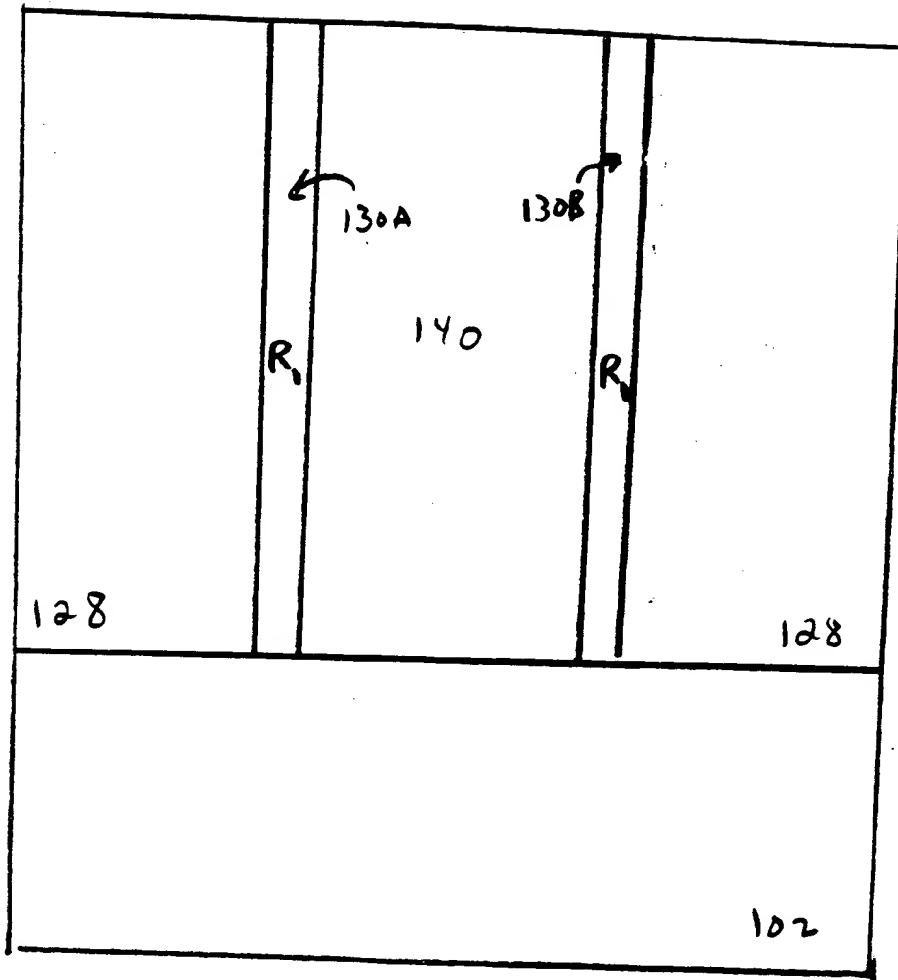


FIGURE 2A



The diagram illustrates a memory array layout. It features a central rectangular region labeled 140. This central region is flanked by two vertical strips, each labeled R<sub>1</sub>. Above the central region, there are two arrows pointing downwards, each labeled 150. To the left of the first R<sub>1</sub> strip, there is a label 130A with an arrow pointing to the strip. To the right of the second R<sub>1</sub> strip, there is a label 130B with an arrow pointing to the strip. The entire structure is enclosed within a larger rectangular frame. The bottom-left corner of the frame is labeled 128, and the bottom-right corner is labeled 102.

FIGURE 2B'



The diagram illustrates a memory array structure. It consists of two columns of memory cells, labeled 130A and 130B. Each column contains two rows of cells, labeled R<sub>1</sub> and R<sub>2</sub>. The cells are connected to word lines 132 and bit lines 140. The array is divided into two sections, 128 and 102, by a vertical line. The word lines 132 are connected to the R<sub>2</sub> cells, and the bit lines 140 are connected to the R<sub>1</sub> cells. The array is also connected to a power supply 160.

200 D'

FIGURE 2D'



A perspective view of a cylindrical container 330' resting on a rectangular base 102. The container has two vertical tubes protruding from its top surface, both labeled 350. The base of the container is indicated by a dashed line.

FIGURE 3B

FIGURE 4A

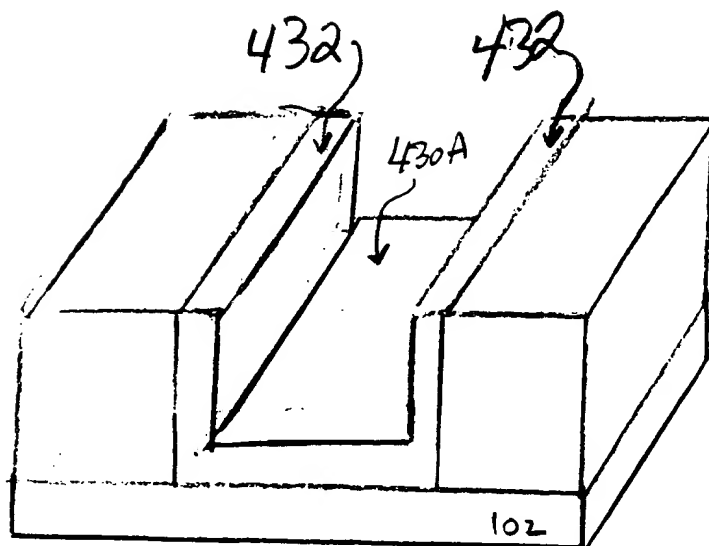


FIGURE 4B

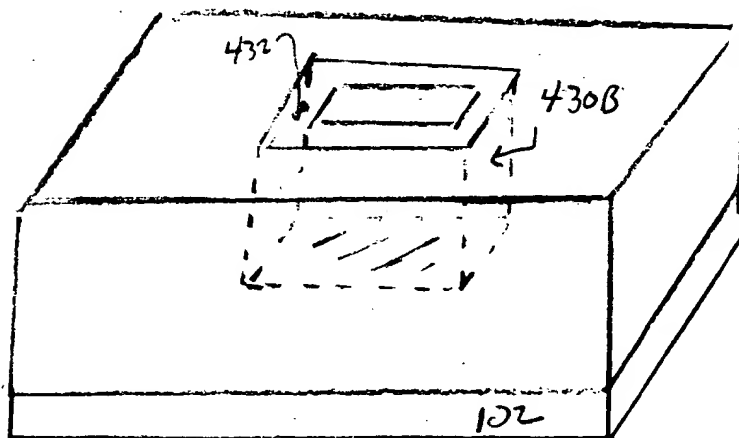
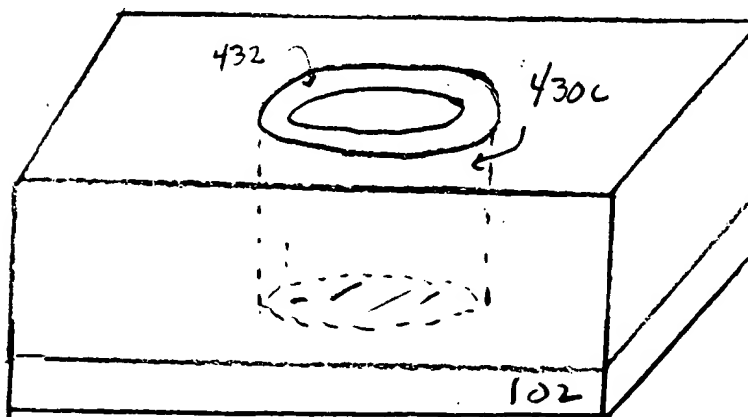


FIGURE 4C



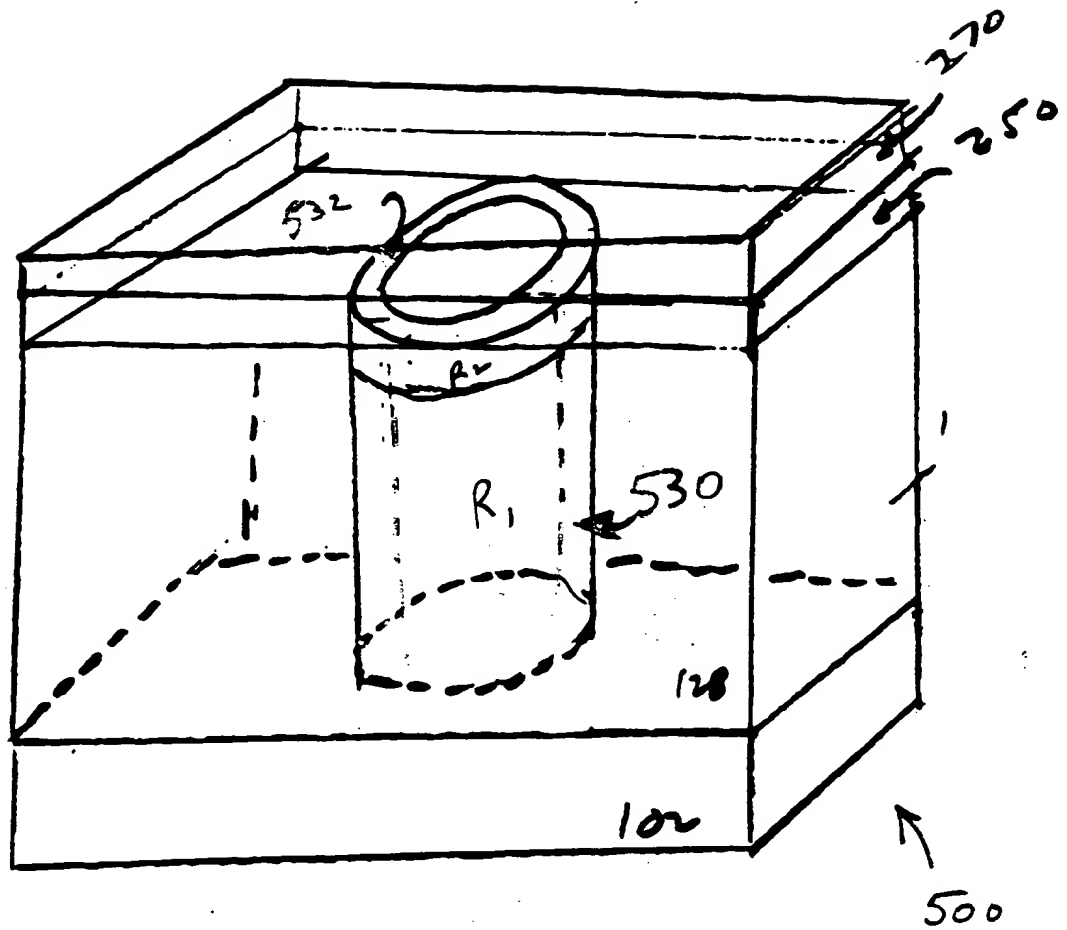


Figure 5A

09620348.07200

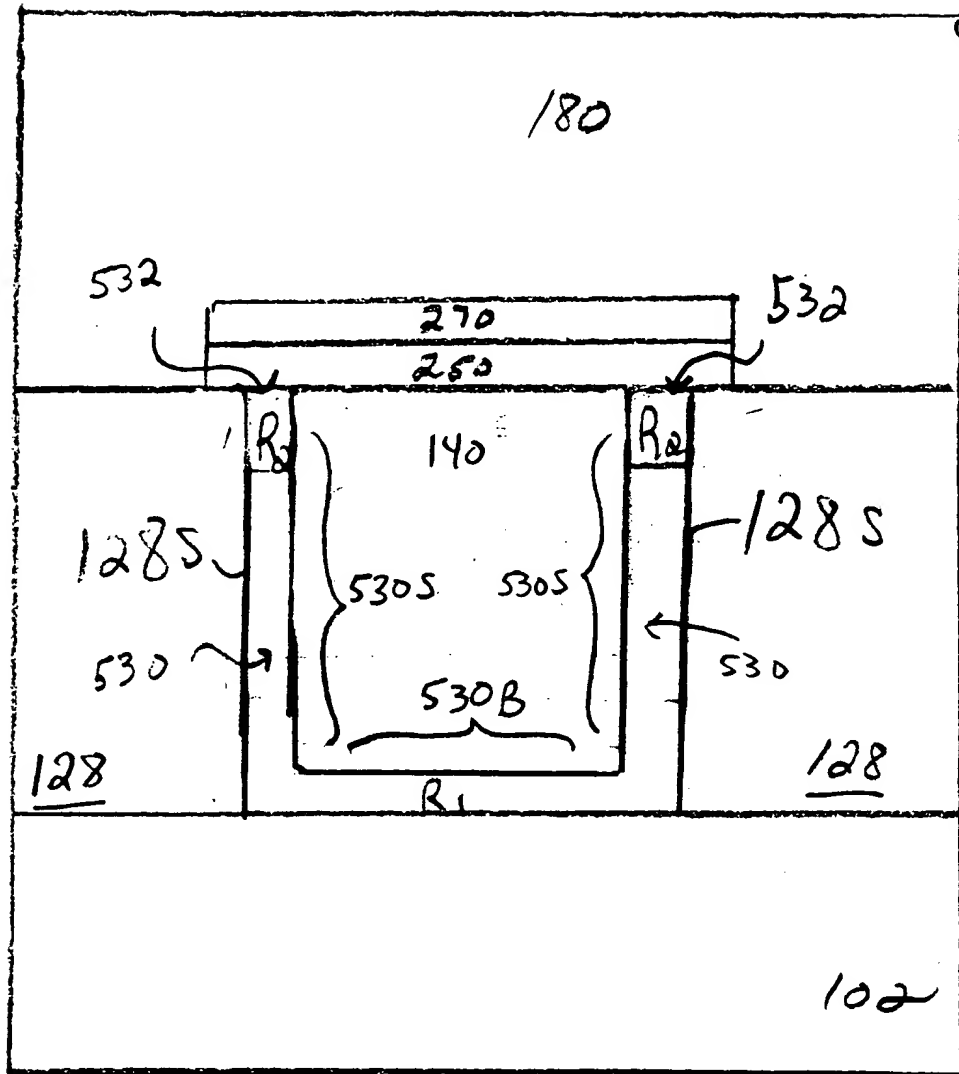


FIGURE 5B



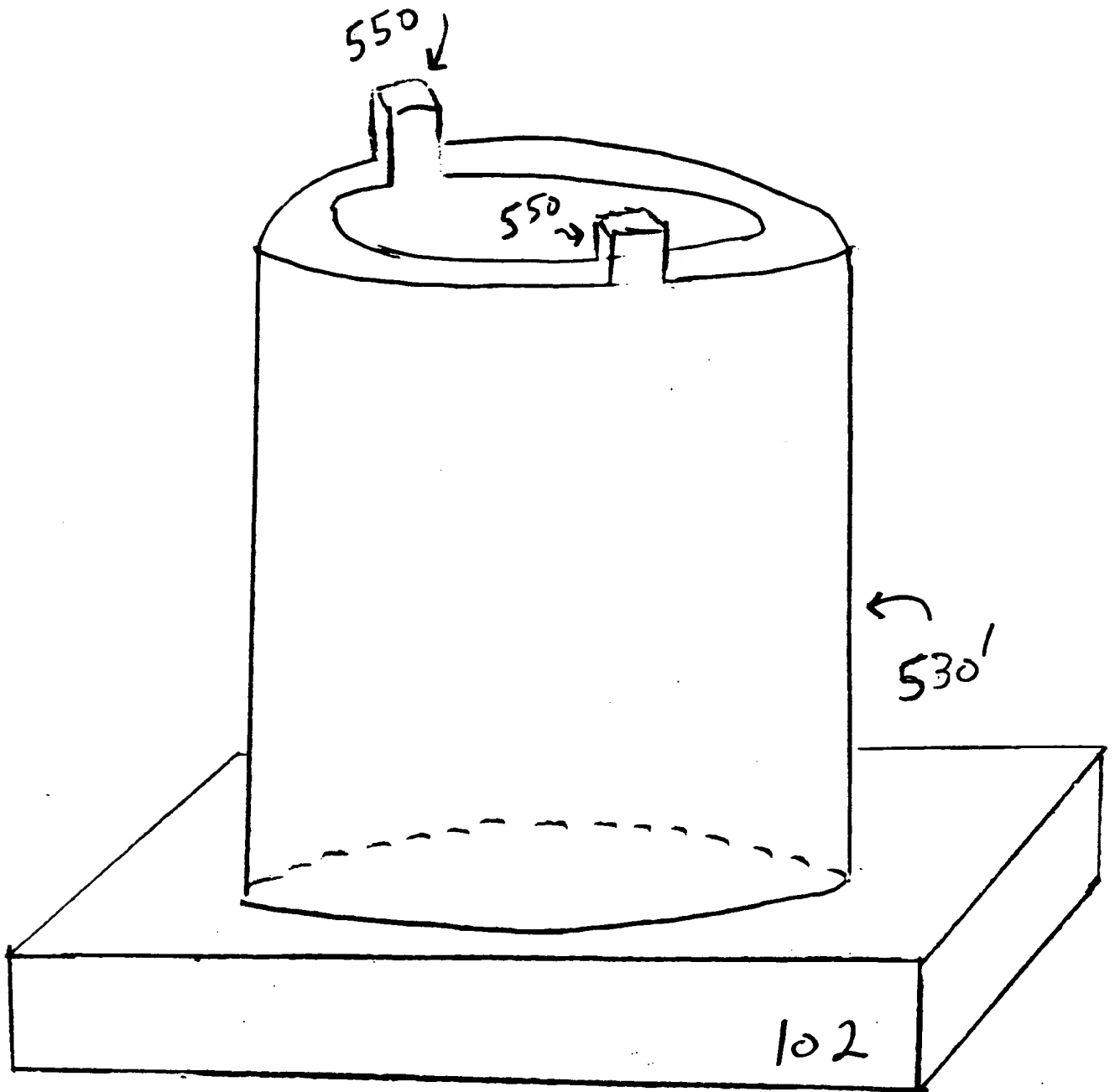
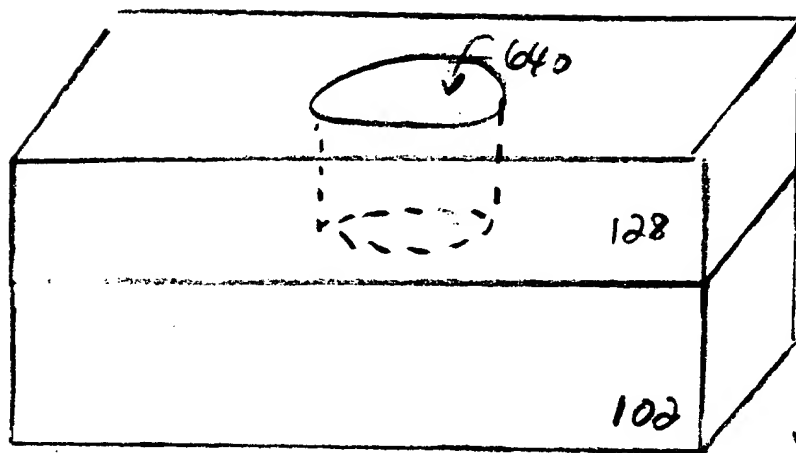
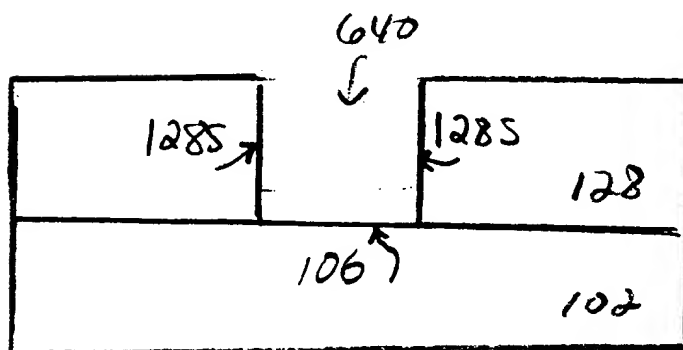


FIGURE 5C



6A

600A



6B

600A

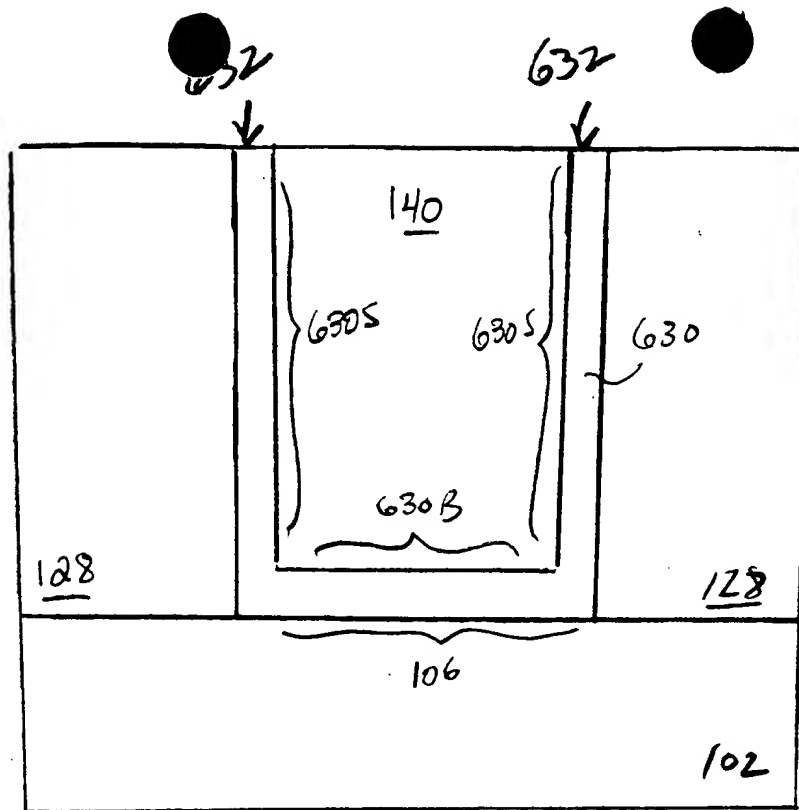
09620348 072200

Hand-drawn schematic diagram of a memory architecture. The diagram shows two main memory blocks, each labeled "633T" at the top and "128" at the bottom. Between these blocks is a central section labeled "640" with a downward arrow. This central section contains a bracketed area labeled "633S" and "633B". To the right of the central section is another block labeled "633". Below the two main blocks is a large section labeled "106" and "102".

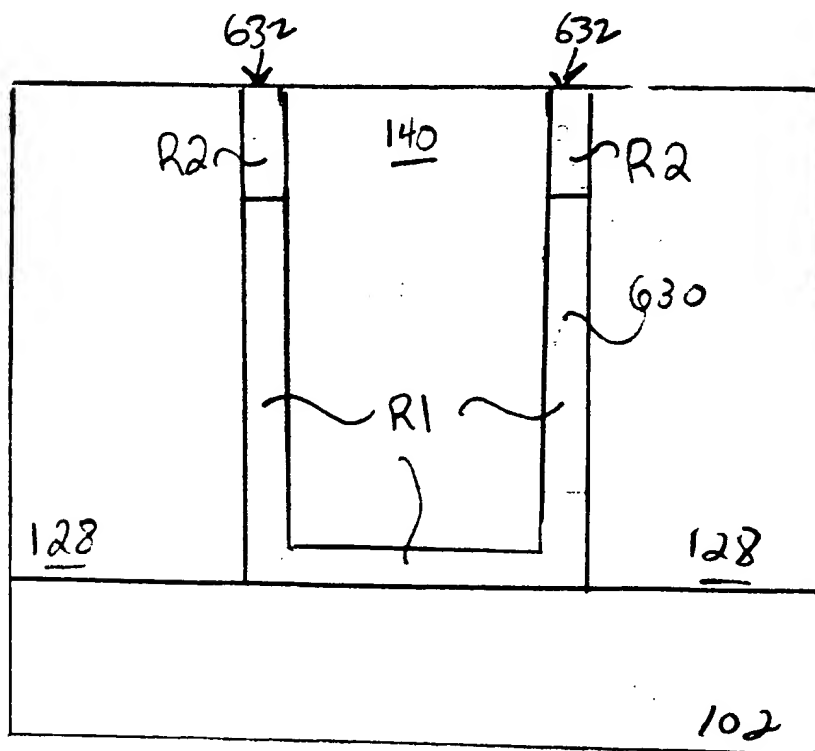
6c

A hand-drawn schematic diagram of a device layout. The diagram shows a central rectangular region labeled 140 at the top. This central region is flanked by two larger rectangular regions, each labeled 633T at the top. Inside each 633T region, there is a smaller rectangular area labeled 128T with an upward-pointing arrow. Below the 128T areas, there are labels 633 with lines pointing to the boundaries. In the center, between the two 633T regions, there is a bracketed area containing labels 633S and 633B. At the bottom of the entire structure, there is a bracketed area labeled 106. The number 128 appears at the bottom left and bottom right corners of the main structure. The number 102 is written at the bottom right of the page.

Good



6E



6F



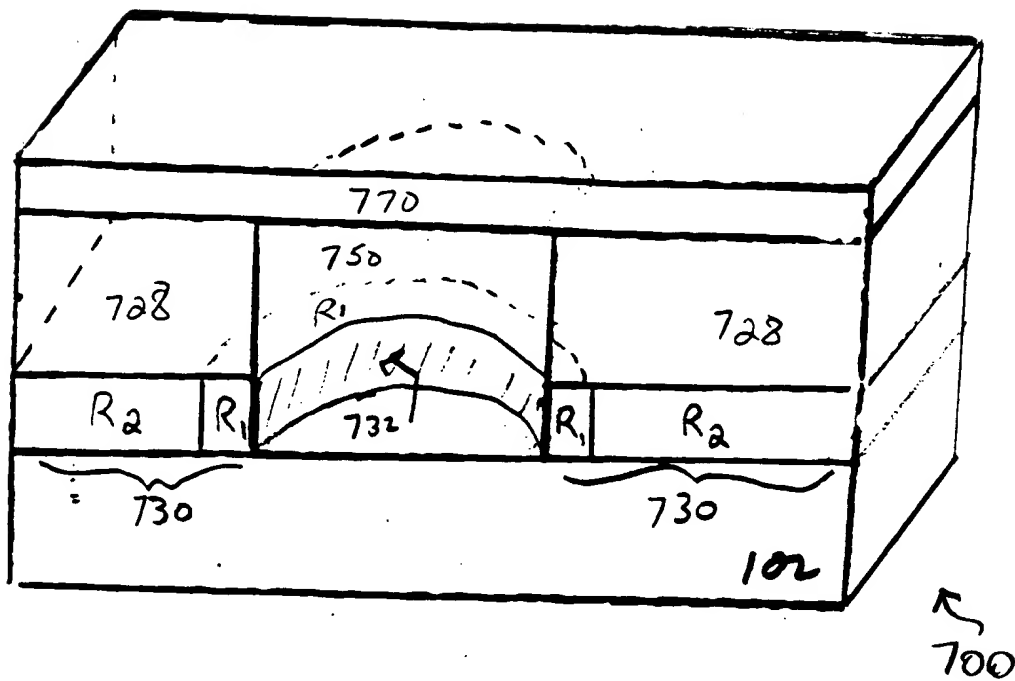


FIGURE 7A

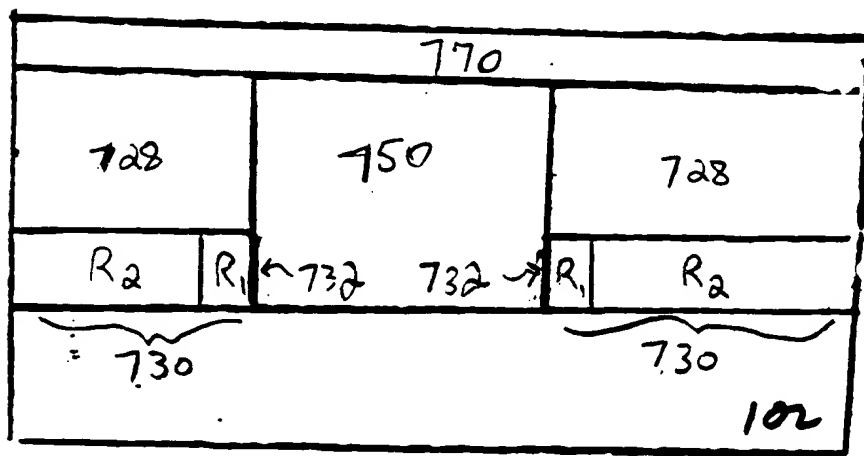


Figure 7B